Docket No.: 57454-257 PATENT

OIPE JC34 JUN 10 2003 PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	
Fukashi MORISHITA	:	
Serial No.: 09/987,566	:	Group Art Unit: 2816
Filed: November 15, 2001	:	Examiner: D. Cunningham

For: INTERNAL POWER SUPPLY VOLTAGE GENERATION CIRCUIT THAT CAN SUPPRESS REDUCTION IN INTERNAL POWER SUPPLY VOLTAGE IN NEIGHBORHOOD OF LOWER LIMIT REGION OF EXTERNAL POWER SUPPLY VOLTAGE

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SUPPLEMENTAL APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Appeal Brief accompanies a Request for Reinstatement of the Appeal filed in response to reopening of prosecution in the Office Action mailed March 12, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Mitsubishi Denki Kabushiki Kaisha, the assignee of the entire right, title and interest in and to the above-identified U. S. Application.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known to the Appellant, which will directly affect or

be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 19 and 20 are pending. Claims 21 and 22 are cancelled. Claims 19 and 20 stand under final rejection, from which rejection this appeal is taken.

IV. STATUS OF AMENDMENTS

No amendment was made after the final Office Action of March 12, 2003. The Advisory Action mailed October 21, 2002 and the Office Action mailed March 12, 2003 do not indicate the status of the amendment under 37 CFR 1.116 filed on October 8, 2002. However, during a telephone conference of October 29, 2002, Examiner Cunningham advised the Applicant's representative that the Amendment under 37 CFR 1.116 filed on October 8, 2002 will be entered for the purposes of Appeal.

V. SUMMARY OF INVENTION

The present invention relates to an internal voltage generating circuit for generating an internal voltage based on a reference voltage. As shown, for example, in FIG. 1 of the drawings, the internal voltage generating circuit may include a reference voltage generation circuit RG for producing reference voltage Vref that determines a level of internal voltage IntVcc developed by the internal voltage generating circuit supplied with external power supply voltage ExtVcc. In particular, the claimed invention is directed to level detection circuitry, such as lower limit detection circuit 1a shown, for example, in FIGS. 4 and 10 of the drawings. As described on pages 31-36 and 47-52 of the specification and recited in claim 19, the level detection circuitry

for detecting a difference between the external power supply voltage ExtVcc and the reference voltage Vref comprises a differential stage including a pair of insulated gate transistors, such as n channel MOS transistors N20 and N21 (FIG. 4) or N20 and N30 (FIG. 10).

The gate of the insulated gate transistor N20 receives the external power supply voltage ExtVcc, whereas the gate of the transistor N21 or N30 receives the reference voltage Vref. One of the conduction nodes of transistor N20 is connected to one of the conduction nodes of transistor N21 or N30. The second conduction node NDC of transistor N20 is provided for outputting a difference signal corresponding to the difference between the external power supply voltage ExtVcc and the reference voltage Vref.

As shown in FIG. 10 and described on pages 47-48 of the specification, the insulated gate transistor N30 has a current supply ability different from a current supply ability of the insulated gate transistor N20.

As specifically recited in claim 19 and described in the specification in connection, for example, with the structure in FIG. 1, the reference voltage Vref determines a level of the internal voltage IntVcc generated from the external power supply voltage ExtVcc.

The level detection circuitry further comprises operation current supply circuitry for supplying an operation current to the insulated gate transistors N20 and N21 (or N30). This operation current supply circuitry comprises a current mirror, such as a current mirror formed by p-channel transistors P20 and P21, coupled to the transistors N20 and N21 (or N30) for supplying current to these transistors.

In addition, the level detection circuitry comprises a buffer circuit, such as a buffer circuit 1ab (FIGS. 4 and 10), for buffering the difference signal to generate a binary level detection signal indicating whether the external power supply voltage ExtVcc is higher than the reference

voltage Vref.

Hence, in accordance with the claimed invention, a power supply voltage is compared with a reference voltage that determines a level of the internal voltage generated based on that power supply voltage. As a result, a stable internal voltage can be generated over an entire operating range of the power supply voltage, even in a lower region of this range, where a difference between the power supply voltage and the internal voltage becomes smaller and the gain of the internal voltage generating circuit is reduced making it impossible to accurately generate the internal voltage based on comparison between the power supply voltage and the internal voltage.

By comparing the power supply voltage with the reference voltage, the claimed arrangement prevents the internal voltage from becoming excessively low in the lower region of the power supply voltage's operating range.

VI. ISSUES

Whether claims 19 and 20 are anticipated by Bion et al. (5,862,091) under 35 U.S.C. 102(e).

VII. GROUPING OF CLAIMS

The rejection under 35 U.S.C. 102(e) applied by the Examiner relates to a group composed of claims 19 and 20.

VIII. THE ARGUMENT

Independent claim 19 recites level detection circuitry for detecting a difference between a

first voltage and a second voltage. The circuitry comprises a differential stage including a first insulated gate transistor and a second insulated gate transistor. The first insulated gate transistor receives a power supply voltage as the first voltage at a gate thereof and has a first conduction node, and a second conduction node for outputting a difference signal. The second insulated gate transistor receives a reference voltage as the second voltage at a gate thereof and having a first conduction node connected to the first conduction node of the first insulated gate transistor. The second insulated gate transistor has a current supply ability different from a current supply ability of the first insulated gate transistor under a condition of the same gate voltage. The difference signal corresponds to a difference between the first and second voltages. The reference voltage determines a voltage level of an internal voltage generated from the power supply voltage.

Also, the level detection circuitry comprises:

-operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, the operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

-a buffer circuit for buffering the difference signal for generating a binary level detection signal indicating whether the first voltage is higher than the second voltage.

The Examiner considers:

-the inverting input of amplifier 37 (FIG. 11 of Bion et al.), or gate of transistor 40 (FIG. 12) to corresponds to the claimed first voltage,

-the non-inverting input of 37 or gate of transistor 39 to correspond to the claimed second voltage,

-the transistor 40 to correspond the claimed first insulted gate transistor,

-the transistor 39 to correspond to the claimed second insulated gate transistor,

-"Vcc, provided by way of transistor 36" to correspond to the claimed power supply voltage,

-"the internal voltage generated from said power supply Vcc, provided to the non-inverting input of 37 by way of resistor-connected transistor 38" to correspond to the claimed reference voltage,

-the transistors 39 and 40 to correspond to the claimed operation current supply, and

-the amplifier 44 to correspond to the claimed buffer circuit.

Considering the reference, FIG. 11 of Bion et al. shows a read circuit 35 having p blocks 34. The outputs of the blocks 34 are connected to the drain of a precharging transistor 36, which is coupled to the inverting input of a differential amplifier 37. The inverting input of this transistor is connected to the drain of a reference transistor 38 which is identical to the precharging transistor 38. The source of the reference transistor 38 is connected to the supply voltage Vcc, and its gate is grounded so as to always maintain transistor 38 in an on condition.

The output of the comparator 37 corresponds to the output of the read circuit 35. The comparator 37 receives a voltage through transistor 38 at its non-inverting input, in order to compensate for the voltage drop via the precharging transistor 36 at the data read out node (corresponding to the inverting input).

Hence, the output of the comparator 37 does not produce a difference signal corresponding to a difference between the power supply voltage Vcc and the reference voltage produced from the power supply voltage Vcc. Instead, the output of 37 produces the read out data supplied to the inverting input. The voltage drop at the precharging transistor 36 (at the inverting input) is compensated by the voltage drop at the identical reference transistor 38 (at the

non-inverting input). Moreover, it is noted that the transistor 38 is employed to compensate for the voltage drop at the precharging transistor 36 that precharges the inverting input, which is not precharged to a power supply voltage level.

Accordingly, the reference does not disclose the claimed differential stage producing a difference signal corresponding to a difference between a power supply voltage and a reference voltage that determines a voltage level of an internal voltage generated from the power supply voltage, as claim 19 requires.

Further, the transistor 38 is employed for compensating for the voltage drop at the precharging transistor 36 to maintain the voltages at non-inverting and inverting input nodes of the comparator at the same voltage level in the standby state. Then, a memory cell is selected, and the comparator determines whether the precharge node is discharged by the comparator, and memory cell data is read out in accordance with the result of this determination.

Therefore, if the reference voltage at the non-inverting input corresponded to the internal voltage, as the Examiner contends, then the both inputs of the comparator 37 would receive the same internal voltage, and the comparison with the power supply voltage would not be performed.

Further, as discussed above, Bion et al. does not disclose a detection signal indicating whether the power supply voltage is higher than the reference voltage that determines the internal voltage generated from the power supply voltage.

Therefore, Bion et al. cannot disclose the claimed buffer circuit for buffering the difference signal for generating a binary level detection signal indicating whether the first voltage is higher than the second voltage.

In response to these arguments presented in the Appeal Brief filed on January 13, 2003,

the Examiner takes the position that the "arguments deal with comparison of the "power supply voltage" and the "reference voltage", however, the claims only recites the comparisons as only being between the "first voltage" and the "second voltage."

The Examiner's position is respectfully traversed. Claim 19 clearly recites "receiving a power supply voltage as the first voltage" and "receiving a reference voltage as the second voltage". The claim also recites that the reference voltage determines a voltage level of an internal voltage generated from the power supply voltage.

Accordingly, claim 19 requires the claimed difference signal corresponding to a difference between the first and second voltages to represent a difference between the power supply voltage and the reference voltage, where the reference voltage determines a voltage level of an internal voltage generated from said power supply voltage.

However, as discussed above, the output of the comparator 37 does not produce a difference signal corresponding to a difference between the power supply voltage Vcc and the reference voltage produced from the power supply voltage Vcc.

Therefore, the reference does not disclose the claimed differential stage producing the difference signal required by claim 19.

Further, as the claim 19 recites "receiving a power supply voltage as the first voltage" and "receiving a reference voltage as the second voltage," the claim requires the claimed binary level detection signal "indicating whether said first voltage is higher than said second voltage" to indicate whether the power supply voltage is higher than the reference voltage that determines the internal voltage generated from the power supply voltage.

However, the amplifier 44 of Bion does not produce a detection signal indicating whether the power supply voltage is higher than the reference voltage that determines the internal

voltage generated from the power supply voltage, as claim 19 requires.

Therefore, the reference does not disclose the claimed buffer circuit for buffering the difference signal required by claim 19 for generating a binary level detection signal prescribed by claim 19.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989). The term "anticipation," in the sense of 35 U.S.C. 102, has acquired the accepted definition meaning "the disclosure in the prior art of a thing substantially identical with the claimed invention." ***In re Schaumann***, 572 F.2d 312, 197 USPQ 5 (CCPA 1978).

However, as demonstrated above, Bion et al. neither expressly nor under principles of inherency describes the differential stage and buffer circuit in the manner required by claim 19.

Therefore, Bion et al. does not anticipate the invention recited in claim 19 within the meaning of 35 U.S.C. 102.

Claim 20 dependent from claim 19 is defined over the reference at least for the reasons presented above in connection with claim 19.

IX. CONCLUSION

For the reasons advanced above, Appellant respectfully contends that the rejection of claims 19 and 20 as being anticipated under 35 U.S.C. § 102 is improper as the Examiner has not met the burden of establishing a *prima facie* case of anticipation. Reversal of the rejection in this appeal is respectfully requested.

Respectfully submitted,

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X. APPENDIX

19. Level detection circuitry for detecting a difference between a first voltage and a second voltage, comprising:

a differential stage including a first insulated gate transistor and a second insulated gate transistor,

said first insulated gate transistor receiving a power supply voltage as the first voltage at a gate thereof and having a first conduction node, and a second conduction node for outputting a difference signal, and

said second insulated gate transistor receiving a reference voltage as the second voltage at a gate thereof and having a first conduction node connected to said first conduction node of said first insulated gate transistor, said second insulated gate transistor having a current supply ability different from a current supply ability of said first insulated gate transistor under a condition of the same gate voltage, and said difference signal corresponding to a difference between the first and second voltages, said reference voltage determining a voltage level of an internal voltage generated from said power supply voltage;

operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, said operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

a buffer circuit for buffering said difference signal for generating a binary level detection signal indicating whether said first voltage is higher than said second voltage.

20. The level detection circuitry according to claim 19, wherein said first insulated gate transistor is smaller in channel width than said second insulated gate transistor.